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TITLE OF INVENTION
LIGHT-EMITTING THYRISTOR AND SELF-SCANNING LIGHT-EMITTING DEVICE

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DESCRIPTION

LIGHT-EMITTING THYRISTOR AND SELF-SCANNING LIGHT-EMITTING DEVICE

TECHNICAL FIELD

The present invention relates to a light-emitting thyristor whose luminous efficiency is improved and a self-scanning light-emitting device using such light-emitting thyristors.

BACKGROUND ART

A surface light-emitting thyristors has been disclosed in the Japanese Patent Publication No. 2-14584, and an end-surface light-emitting thyristor in the Japanese Patent Publication No. 9-85985. The fundamental structure of a surface light-emitting thyristor and that of a end-surface light-emitting are substantially the same, and AlGaAs (Al composition is 0.35, for example) layers are epitaxially grown on a GaAs buffer layer formed on a GaAs substrate, for example.

Fig.1 is a schematic cross-sectional view depicting a fundamental structure of a light-emitting thyristor. As shown in Fig.1, on a p-type GaAs substrate 10 successively stacked are a p-type GaAs buffer layer 12, a p-type AlGaAs layer 14, an n-type AlGaAs layer 16, a p-type AlGaAs layer 18, and an n-type AlGaAs layer 20. On the AlGaAs layer 20 provided is a cathode electrode 22, and on the AlGaAs layer 18 a gate electrode 24. An anode electrode 26 is provided on the bottom surface of the GaAs substrate 10.

In this example, a p-type layer, an n-type layer, a p-

type layer, and an n-type layer are stacked in this order on a p-type GaAs substrate via a buffer layer. However, an n-type layer, an p-type layer, an n-type layer, and a p-type layer may be stacked in this order on an n-type GaAs substrate via a buffer layer, in this case the uppermost electrode is an anode one, and the bottommost electrode is a cathode one.

In the above-described publications, the inventors of this application have already disclosed a self-scanning light-emitting device structured by arranging such light-emitting thyristors in an array, a self-scanning function thereof being implemented by providing a suitable interaction between neighbored thyristors in the array. The publications have further disclosed that such self-scanning light-emitting device has a simple and compact structure for a light source of a printer, and has smaller arranging pitch of thyristors in the array.

In the light-emitting thyristor having such structure described-above, Al composition is largely varied, for example from 0 to 0.35, at the interface between the GaAs buffer layer and the AlGaAs layer on the buffer layer. Such rapid variation of Al composition causes the turbulence of lattices or the large variation of energy bands at the interface, while the variation of lattice constants is small. As a result, a lattice-mismatching at the interface become large, thereby causing a dislocation. Also, an energy gap at the interface is increased, so that the deformation of energy bands is made large.

Therefore, for the light-emitting thyristor fabricated by growing the AlGaAs layer on the GaAs substrate interposing

the GaAs buffer layer therebetween, there are problems such that a device property is degraded due to the increase of a threshold current and a holding current. This is because lattice deffects due to a lattice-mismatching at the interface between the GaAs buffer layer and the AlGaAs layer are induced, and an unclear impurity level is formed at the interface. There are also problems such that an external quantum efficiency is decreased, resulting in the reduction of the amount of emitted light. This is because defects which serve as "carrier killers" are generated in the vicinity of the interface.

As shown in Fig.2 wherein like elements are indicated by like reference numerals used in Fig.1, an n-type GaAs layer 28 may be provided on an n-type AlGaAs layer 20 in a conventional light-emitting thyristor. In this manner, GaAs is used as the material of the uppermost layer for the facility of making ohmic contact with an electrode and the simplicity of material. Since the wave length of emitted light is about 780nm, the light is absorbed during passing through the uppermost layer (GaAs layer) 28 so that the amount of light to be emitted is decreased.

In order to reduce the light absorption by the GaAs layer 28, the thickness of the layer is needed to be thinner. However, if the layer is thinner, additional problems are caused. That is, alloying of electrode material and GaAs by a heat processing is required to from an ohmic electrode, and atoms migrate for a long distance during the heat processing, as a result of which the alloyed area of electrode material is reached to the AlGaAs layer 20 under the GaAs layer 28. This causes the turbulence of crystalline of AlGaAs,

resulting in the scattering of light.

Fig.3 is a graph showing a light absorption spectrum of an n-type GaAs layer at 297K, wherein ordinate designates an absorption coefficient α and abscissa a photon energy. The amount of absorbed light is represented by the following formula.

$1-e^{-\alpha t}$ (t ; film thickness)

It is noted from this graph that the absorption coefficient for the light of 780nm wave length is about 1.5×10^4 . Assuming that the film thickness "t" is 0.02μm, it is understood that the amount of emitted light is decreased by 3-4% by calculating the amount of absorbed light based on the above formula. The amount of absorbed light will be further reduced, if the turbulence of atomic arrangement is caused due to the fluctuation of film thickness and the alloying, and the variation of composition.

Fig.4 shows a light-emitting thyristor in which a GaAs buffer layer 12 is provided on a GaAs substrate 10, and a GaAs layer 28 is used as a topmost layer. In the figure, like element are indicated by like reference numerals used in Figs.1 and 2.

In general, a light-emitting thyristor having a pnpn structure is considered to be the combination of a pnp transistor 44 on the substrate side and an npn transistor 46 on the opposite side to the substrate, as shown in Fig.5. An anode corresponds to an emitter of the pnp transistor 44, a cathode an emitter of the pnp transistor 46, and a gate a base of the pnp transistor 46, respectively. The holding current of the thyristor is determined by the combination of current amplification factors of respective transistors 44

and 46. In order to decrease the holding current, it is required to increase current amplifying factors α of respective transistors. A current amplifying factor α is given by the multiplication of an emitter injection efficiency γ, a transport efficiency β, a collector junction avalanche multiplication factor M, and a specific collector efficiency α^*. In order to increase an emitter injection efficiency γ, the impurity concentration of the emitter is designed to be higher that of the base.

The diffusion speed of Zn which is a p-type impurity is very fast, so that Zn is diffused into an n-type semiconductor layer to compensate an n-type impurity. Therefore, if Zn concentration of the anode layer (the GaAs layer 12 and the AlGaAs layer 14) is higher than Si impurity concentration of the n-type gate layer (the AlGaAs layer 16), then most of Si in the vicinity of the interface between the anode layer and the gate layer is compensated to decrease a transport efficiency β of the transistor. Also, non-luminescent center is generated, causing the reduction of the luminous efficiency of the thyristor.

DISCLOSURE OF INVENTION

An object of the present invention is to provide a light-emitting thyristor in which the luminous efficiency thereof is improved, the thyristor being fabricated by growing AlGaAs layers on a GaAs buffer layer formed on a GaAs substrate.

Another object of the present invention is to provide a light-emitting thyristor using GaAs for the material of the uppermost layer, in which the luminous efficiency thereof is

improved.

Still another object of the present invention is to provide a light-emitting thyristor including Zn impurity in an n-type gate layer, in which the luminous efficiency thereof is improved.

A further object of the present invention is to provide a self-scanning light-emitting device using such light-emitting thyristors.

An aspect of the present invention is a light-emitting thyristor in which a p-type AlGaAs layer and an n-type AlGaAs layer are alternately stacked to form a pnpn structure on a GaAs buffer layer formed on a GaAs substrate. Al composition of the AlGaAs layer on the GaAs buffer layer is increased in steps or continuously.

According to this light-emitting thyristor, an Al composition of said AlGaAs layer is gradually varied, so that the lattice defects such as dislocation due to lattice-mismatching at the interface between the GaAs buffer layer and the AlGaAs layer may be decreased, and the extreme deformation of an energy band at the interface may be softened.

It is also useful that a single or multi quantum well layer, or a strained superlattice structure is inserted in place of gradual variation of Al composition. In this case, if a quantum well layer or a superlattice layer having a high reflectivity is used, the light toward the substrate is reflected by the quantum well layer or the superlattice layer, thus increasing the amount of emitted light.

When a misfit dislocation is caused in the AlGaAs layer in which Al composition is varied in steps or continuously, a

quantum well layer or a strained superlattice structure may be inserted into the AlGaAs layer in order to block the propagation of the misfit dislocation.

According to a second aspect of the present invention, the light absorption by the topmost layer may be decreased by utilizing a material such as InGaP, InGaAsP, or AlGaInP having a absorption edge wave length shorter than 780nm. It is desirable that this material is lattice matched with the GaAs substrate. As a result, an external quantum efficiency may be increased because the light absorption by the topmost layer is decreased.

According to a third aspect of the present invention, an impurity concentration of at least a part of an anode layer near an n-type gate layer is lower than an impurity concentration of the n-type gate layer in a pnpn structure light-emitting thyristor. Where a p-type first layer, a p-type second layer, an n-type third layer, a p-type fourth layer, an n-type fifth layer, and an n-type sixth layer are epitaxially grown on a p-type substrate, for example, such light-emitting thyristor is composed of the combination of a pnp transistor on the substrate side and an npn transistor on the opposite side to the substrate.

According to the present invention, each impurity concentration of the first and second layer is equal to or smaller than that of the third layer to limit a impurity diffusion from the first and second layer to the third layer. Since an emitter-base junction of a pnp transistor is a hetero junction, even if an impurity concentration of an emitter is lower than that of a base, an emitter injection efficiency is not affected and is held to about 1.

Using light-emitting thyristors described above, a self-scanning light-emitting device of the following structure may be implemented.

A first structure of the self-scanning light-emitting device comprises a plurality of light-emitting elements each having a control electrode for controlling threshold voltage or current for light-emitting operation. The control electrodes of the light-emitting elements are connected to the control electrode of at least one light-emitting element located in the vicinity thereof via an interactive resistor or an electrically unidirectional element, and a plurality of wirings to which voltage or current is applied are connected to electrodes for controlling the light emission of light-emitting elements.

A second structure of the self-scanning light-emitting device comprises a self-scanning transfer element array having such a structure that a plurality of transfer elements each having a control electrode for controlling threshold voltage or current for transfer operation are arranged, the control electrodes of the transfer elements are connected to the control electrode of at least one transfer element located in the vicinity thereof via an interactive resistor or an electrically unidirectional element, power-supply lines are connected to the transfer elements by electrical means, and clock lines are connected to the transfer elements; and a light-emitting element array having such a structure that a plurality of light-emitting elements each having a control electrode for controlling threshold voltage or current are arranged, the control electrodes of the light-emitting element array are connected to the control electrodes of said

transfer elements by electrical means, and lines for applying current for light emission of the light-emitting element are provided.

According to the structures described above, an increased luminous efficiency, high-density, compact and low-cost self scanning light-emitting device may be implemented.

BRIEF DESCRIPTION OF DRAWINGS

Fig.1 is a schematic cross-sectional view of a conventional light-emitting thyristor having a buffer layer.

Fig.2 is a schematic cross-sectional view of a conventional light-emitting thyristor using a GaAs layer as a topmost layer.

Fig.3 is a graph showing a light absorption spectrum of an n-type GaAs layer.

Fig.4 is a schematic cross-sectional view of a conventional light-emitting thyristor.

Fig.5 is an equivalent circuit diagram of the thyristor shown in Fig.4.

Fig.6 is a schematic diagram showing a first embodiment of the present invention.

Fig.7 is a schematic diagram showing a second embodiment of the present invention.

Fig.8 is a circuit diagram of a characteristic estimating circuit for a light-emitting thyristor.

Fig.9 is a graph showing a measured threshold current.

Fig.10 is a graph showing a measured holding current.

Fig.11 is a schematic diagram showing a third embodiment of the present invention.

Figs.12 and 13 are schematic diagrams showing a fourth

embodiment of the present invention.

Fig.14 is a schematic diagram showing a fifth embodiment of the present invention.

Fig.15 is a graph showing a photoluminescence intensity of InGaP.

Fig.16 is a graph showing a light absorption spectrum of $In_{0.5}Ga_{0.5}P$ layer.

Fig.17 is a circuit diagram of a light output measuring circuit.

Fig.18 is a composition diagram of InGaAs.

Fig.19 is a graph illustrating the relationship between a lattice constant and an energy gap of AlGaInP.

Fig.20 is a graph showing current-light output characteristics.

Fig.21 is a schematic diagram showing a seventh embodiment of the present invention.

Fig.22 is an equivalent circuit diagram of a first fundamental structure of the self-scanning light-emitting device.

Fig.23 is an equivalent circuit diagram of a second fundamental structure of the self-scanning light-emitting device.

Fig.24 is an equivalent circuit diagram of a third fundamental structure of the self-scanning light-emitting device.

BEST MODE FOR CARRYING OUT THE INVENTION

The embodiments of the present invention will now be described with reference to drawings.

First Embodiment

Referring to Fig.6, there is shown an embodiment of the present invention wherein the problems in the conventional thyristor shown in Fig.1 may be resolved. In Fig.6, $Al_xGa_{1-x}As$ layer is epitaxially grown on a GaAs substrate 10 in such a manner that Al composition x is increased in steps from 0 (GaAs) to 0.35. Since the method of epitaxial growth is identical independent of the types of conductivity (n-type or p-type) of GaAs and AlGaAs, the embodiment will be illustrated without distinguishing the conductivity type.

AlGaAs layer is epitaxially grown on the GaAs buffer layer 12 by varying the supply flow rate of Al in such a manner that Al composition is varied at 0, 0.1, 0.2, 0.3, 0.35, for example. That is, a GaAs layer 12 having Al composition of 0, an AlGaAs layer 50-1 having Al composition of 0.1, an AlGaAs layer 50-2 having Al composition of 0.2, an AlGaAs layer 50-3 having Al composition of 0.3, and an AlGaAs layer 50-4 having Al composition of 0.35 are epitaxially grown successively.

Four AlGaAs layers 50-1, 50-2, 50-3 and 50-4 that Al compositions are increased in steps correspond to the layer 14 in Fig.1. In this case, the total film thickness from the GaAs buffer layer 12 to AlGaAs layer 50-4 is determined by a containment efficiency of carriers.

The processing steps hereinafter is the same as the conventional steps in Fig.1. Then, AlGaAs layers having Al composition of 0.35, respectively, are epitaxially grown hereinafter.

Second Embodiment

Referring to Fig.7, there is shown a second embodiment

of the present invention wherein the problems in the conventional thyristor shown in Fig.1 is also resolved. In Fig.7, $Al_xGa_{1-x}As$ layer is epitaxially grown on a GaAs buffer layer 12 in such a manner that the composition x of Al is continuously increased from 0 to 0.35. Such modification of Al composition is implemented by varying continuously at least one of supply flow rates of Al and Ga.

In this manner, on the GaAs buffer layer 12 just above the GaAs substrate 10, formed is an AlGaAs layer 52-1 having an Al composition varied from 0 to 0.35, and then an AlGaAs layer 52-2 having an Al composition of 0.35.

These two AlGaAs layers 52-1 and 52-2 are corresponding to the AlGaAs layer 14 in Fig.1. In this case, the total of film thickness from the GaAs buffer layer 12 to AlGaAs layer 52-2 is determined by a containment efficiency of carriers.

The steps hereinafter is the same as the conventional steps in Fig.1. Then, AlGaAs layers having Al composition of 0.35, respectively, are epitaxially grown hereinafter.

According to the present embodiments wherein an Al composition is continuously varied, the lattice defects such as dislocation due to lattice-mismatching at the interface between the GaAs buffer layer and the AlGaAs layer may be decreased, and the extreme deformation of an energy band at the interface may be softened. As a result, an adverse effect with respect to the device characteristic is reduced.

A threshold current, holding current, and light output of the light-emitting thyristors of the first and second embodiments are measured by the following method as illustrated in Fig.8. An anode electrode 62, a cathode electrode 64, and gate electrode 66 of a light-emitting

thyristor 66 are connected to a constant current source 68 and a constant voltage source 70 as shown in Fig.8. In this characteristic estimating circuit, a cathode voltage V_k and a gate current I_g were measured by varying an output current I_k of the constant current source 68. A typical example of measurements is shown in a graph of Fig.9. A maximum current just before the gate current I_g was reversed from up to down was considered as a threshold current. A cathode voltage V_k was also measured by varying the output current I_k which is equal to a cathode current of the thyristor 60. A typical I_k-V_k characteristic is shown in a graph of Fig.10. The holding current was defined as a current wherein the cathode voltage was over a constant value (e.g., 0.2V). The light output in the case when the gate electrode was connected to the anode electrode through a resistor and the output current I_k was set to a suitable value (e.g., 13mA), was measured by a photodiode.

Fifteen-twenty thyristors of the first or second embodiment were measured as to the threshold current, holding current , and light output. Compared with the conventional thyristor shown Fig.1, the threshold current was decreased by about 20% in average, the holding current was decreased by about 15% in average, and the light output was increased by about 10% in average.

Third Embodiment

Referring to Fig.11, there is shown a third embodiment of the present invention wherein the problems in the conventional thyristor shown in Fig.1 is also resolved. In Fig.11, a quantum well layer 72 is formed on the GaAs buffer

layer 12 just above the GaAs substrate 10. On the layer 72, the AlGaAs layer 14, AlGaAs layer 16, ... are epitaxially grown in the same manner as in Fig.1. The quantum well layer 72 serves as same as the AlGaAs layer wherein Al composition is increased in steps in the first embodiment or the AlGaAs layer wherein Al composition is continuously increased in the second embodiment. As a result, the lattice defects such as dislocation due to lattice-mismatching at the interface between the GaAS buffer layer and the AlGaAs layer may be decreased, and the extreme deformation of an energy band at the interface may be softened.

Alternatively, a quantum well layer may be inserted into the AlGaAs layer 14 in place of providing the quantum well layer between the GaAs buffer layer 12 and AlGaAs layer 14. Also, a strained superlattice structure may be used in place of the quantum well layer, resulting in the same effect as that in the quantum well layer.

Fourth Embodiment

In the AlGaAs layer wherein Al composition is varied in steps or continuously, there is a problem in that misfit dislocation caused by lattice-mismatching propagates through the AlGaAs layer and reaches the upper layer, thus adversely affecting the characteristic of the thyristor. Embodiments will now be described in which the propagation of such misfit dislocation is reduced or blocked.

In an embodiment shown in Fig.12, a quantum layer or strained superlattice structure 74 is inserted into the AlGaAs layer 50-4 in Fig.6. The propagation of the misfit dislocation may be blocked by means of the quantum layer or

strained superlattice structure 74.

In an embodiment shown in Fig.13, a quantum layer or strained superlattice structure 76 is inserted into the AlGaAs layer 52-2 in Fig.7. The propagation of the misfit dislocation may be blocked by means of the quantum layer or strained superlattice structure 76.

Fifth Embodiment

Fig.14 is a schematic cross sectional view of a light-emitting thyristor of the present invention, in which the problems in the conventional thyristor using a GaAs layer for a topmost layer as shown in Fig.2 is resolved. The structure of the embodiment is substantially the same as that of the conventional thyristor shown in Fig.2, except that the topmost GaAs layer is replaced by a layer 80 consisting of InGaP which is lattice-matched with the GaAs substrate.

$In_{1-x}Ga_xP$ is lattice-matched with GaAs, when the composition x is about 0.5. When InGaP is grown by means of MOCVD, trimetylindium (TMI) is used for In component, trimetylgallium (TMG) for Ga component, and phosphine for P component. Since the growth conditions of InGaP depend upon the structure of a reactor, the setting of growth conditions is required so as to obtain the desired composition x, i.e., 0.5. A growth temperature is in a range of 600-700℃, when a low pressure growth method is used. Mole ratio (TMG/TMI) of TMG and TMI both of them being material for Ⅲ Group components is determined, assuming that said mole ratio is proportional to a mixed crystal ratio(x/1-x). Selenium is used as a dopant for obtaining an n-type InGaP, hydrogen selenide being utilized for selenium component.

A sample in which a single layer of InGaP was grown on a GaAs substrate was prepared for estimating an optical characteristic. Fig.15 shows a photoluminescence intensity of $In_{0.5}Ga_{0.5}P$ layer measured at a room temperature. A central wave length of emitted light is about 660nm. Fig.16 shows a light absorption spectrum of said $In_{0.5}Ga_{0.5}P$ layer in comparison with that of the GaAs layer shown in Fig.3. The absorption edge wave length of $In_{0.5}Ga_{0.5}P$ is about 650nm (0.9ev) and the absorption coefficient for the light of 780nm wave length is lower than $10cm^{-1}$, which is sufficiently smaller than the absorption coefficient $1.5\times10^{4}cm^{-1}$ of GaAs.

Said InGaP layer is used as the uppermost cathode layer when a light-emitting thyristor is fabricated. The growth method of the InGaP layer is the same way as described above, and the other processes are substantially the same as that has been disclosed as to the thyristor using a GaAs layer. Also, in order that a cathode electrode makes ohmic contact with the InGaP layer, AuGeNi is used for the material of the cathode electrode.

To measure the light output of the thyristor, a constant current source and resistors are connected to the thyristor as shown in Fig.17. The gate electrode 84 is connected to the anode electrode 88 through the resistor 86, and the constant current source 92 is connected between the anode electrode 88 and the cathode electrode 90. The light output of the thyristor was measured under the constant cathode current (e.g., 10mA) by means of a photodiode.

The resulting light output was increased by about 3% in average compared with the typical value of the conventional thyristor. This shows that the light absorption by the

$In_{0.5}Ga_{0.5}P$ layer is negligibly small.

In the case where $In_{1-x}Ga_xAs_{1-y}P_y$ is used for the material of the uppermost layer, an absorption coefficient may be caused to be small by using the compositions x and y on a large absorption end energy side, respectively. For illustrating this, a composition diagram of $In_{1-x}Ga_xAs_{1-y}P_y$ is shown in Fig.18. In the figure, a solid line designates a contour of energy gap Eg, and a dotted line a contour of lattice constant. According to this composition diagram, a line 100 designating an absorption energy of 1.6eV corresponds to a 780nm wave length of emitted light, and a lattice constant of 5.65 Å corresponds to that of GaAs. Therefore, it is apparent from Fig.18 that an absorption coefficient may be decreased by using a composition on a high energy side from the dot 102 within compositions having a lattice constant equal to that of GaAs.

In the case where $Al_xGa_yIn_{1-x-y}P$ is used for the material of the uppermost layer, it is required to select each composition x or y so that $Al_xGa_yIn_{1-x-y}P$ is lattice matched with GaAs. Fig.19 is a graph for illustrating the relationship between a lattice constant and an energy gap of AlGaInP. In the figure, ordinate designates a lattice constant and obscissa an energy gap Eg. A shaded area 104 shows a composition region in which $Al_xGa_yIn_{1-x-y}P$ may be formed, and the composition indicated by a solid line 106 within said composition region is lattice matched with GaAs. In this composition, the energy gap is sufficiently larger with respect to a wave length of 780nm, then an absorption coefficient is considered to be sufficiently smaller compared with that of GaAs.

Sixth Embodiment

The embodiment of the present invention will now be described, in which the problems caused in the conventional thyristor shown in Fig.4.

The light-emitting thyristor was fabricated, in which only each concentration of the p-type GaAs layer 12 and the p-type AlGaAs layer 14 in the structure of Fig.4 was varied. A table 1 shows the kind of material, the film thickness, the type of impurity, and the concentration of impurity of each layer and the substrate.

Table 1

Layer	Material	Thick. (nm)	Impurity	Impurity Concentration (atom/cm^3)			
				No. 1	No. 2	No. 3	No. 4
Layer 28	GaAs	30	Si	3×10^{18}	3×10^{18}	3×10^{18}	3×10^{18}
Layer 20	$Al_{0.3}Ga_{0.7}As$	500	Si	3×10^{18}	3×10^{18}	3×10^{18}	3×10^{18}
Layer 18	$Al_{0.13}Ga_{0.87}As$	800	Zn	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Layer 16	$Al_{0.13}Ga_{0.87}As$	200	Si	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}
Layer 14	$Al_{0.3}Ga_{0.7}As$	500	Zn	2×10^{17}	2×10^{18}	5×10^{17}	1×10^{18}
Layer 12	GaAs	500	Zn	2×10^{17}	2×10^{18}	5×10^{17}	1×10^{18}
Substrate 10	GaAs		Zn				

The substrate 10 is composed of GaAs, and the impurity therein is Zn. The buffer layer 12 is composed of GaAs with 500nm thickness, and the impurity therein is Zn. The anode layer 14 is composed of $Al_{0.3}Ga_{0.7}As$ with 500nm thickness, and the impurity therein is Zn. The n-type gate layer 16 is composed of $Al_{0.13}Ga_{0.87}As$ with 200nm, and the impurity therein is Si. The p-type gate layer 18 is composed of $Al_{0.13}Ga_{0.87}As$ with 800nm thickness, and the impurity therein is Zn. The

cathode layer 20 is composed of $Al_{0.3}Ga_{0.7}As$ with 500nm thickness, and the impurity therein is Si. The ohmic contact layer 28 is composed of GaAs with 30nm thickness, and the impurity therein is Si.

Four types of impurity concentration, i.e., Nos.1-4 were prepared as shown in Table 1. Nos.1-4 impurity concentration in each of the four layers 16, 18, 20, 28 are the same. That is, Si impurity concentration of the layer 16 is $1\times10^{18}/cm^3$, Zn impurity concentration of the layer 18 is $1\times10^{17}/cm^3$, Si impurity concentration of the layer 20 is $3\times10^{18}/cm^3$, and Si impurity concentration of the layer 28 is $3\times10^{18}/cm^3$.

On the other hand, each Zn impurity concentration of the layers 12 and 14 in No.1 is $2\times10^{17}/cm^3$, each Zn impurity concentration of the layers 12 and 14 in No.2 is $2\times10^{18}/cm^3$, each Zn impurity concentration of the layers 12 and 14 in No.3 is $5\times10^{17}/cm^3$, and each Zn impurity concentration of the layers 12 and 14 in No.4 is $1\times10^{18}/cm^3$.

Apparent from the above, each impurity concentration of the layers 12 and 14 is not lower than that Si impurity concentration of the layer 16 in Nos.2 and 4.

For the light-emitting thyristors each having impurity concentration of Nos.1-4, the current-light output characteristics were measured, respectively. The resulting current-light output characteristics are shown in Fig.20. The light-emitting thyristor of No.1 wherein each Zn concentration of the layers 12 and 14 is sufficiently lower than Si concentration of the layer 16 has the highest amount of emitted light. The thyristor of No.3 has the next higher amount of emitted light. On the other hand, the thyristors of No.4 and No.2 wherein each Zn concentration of the layers

12 and 14 is equal to or lower than Si concentration of the layer 16 have the lower amount of emitted light. Therefore, it is noted that the luminous efficiency of the thyristor is not decreased, in which each Zn concentration of the layers 12 and 14 is set so as to be lower than Si concentration of the layer 16. This is because the impurity diffusion from the layers 12 and 14 to the layer 16 is limited.

Seventh Embodiment

In the sixth embodiment described above, it is made apparent that the advantageous effect may be obtained by lowering each impurity concentration of the layers 12 and 14 than that of the layer 16. However, the lowering of each impurity concentration of the layers 12 and 14 increases each resistance of these layers, having an effect on the characteristic of the thyristor. In order to avoid this, the layer 14 in the sixth embodiment is divided into two layers 14-1 and 14-2 as shown in Fig.21. In this thyristor, the impurity concentration of each layer is set as shown in Table 2. The impurity concentration of the upper layer 14-2 of two divided layers is set to lower concentration, i.e., $2 \times 10^{16}/cm^3$, and that of the lower layer 14-1 is set to $2 \times 10^{18}/cm^3$. Each impurity concentration of another layers is the same as in the sixth embodiment.

An impurity concentration of each layer after growing was measured by a secondary ion mass spectroscopy, the result (measured concentration) of which is also shown in Table 2. According to the measuring result, it is noted that the impurity concentration of the upper layer 14-2 was $4 \times 10^{17}/cm^3$ larger than the set concentration ($2 \times 10^{16}/cm^3$). This is

because Zn was diffused from the lower layer 14-1 to the upper layer 14-2 during growing the upper layer.

The current-light output characteristic of the thyristor according to this embodiment was similar to that of No.1 case of the sixth embodiment. Therefore, it is noted that there is an effect when the impurity concentration of the part of the layer 14 near the layer 16 is low.

Table 2

Layer	Material	Thick. (nm)	Impurity	Impurity Concentration (atom/cm^3)	
				Set	Measured
Layer 28	GaAs	30	Si	3×10^{18}	3×10^{18}
Layer 20	$Al_{0.3}Ga_{0.7}As$	500	Si	3×10^{18}	3×10^{18}
Layer 18	$Al_{0.13}Ga_{0.87}As$	800	Zn	1×10^{17}	1×10^{17}
Layer 16	$Al_{0.13}Ga_{0.87}As$	200	Si	3×10^{18}	3×10^{18}
Layer 14-2	$Al_{0.3}Ga_{0.7}As$	100	Zn	2×10^{16}	4×10^{17}
Layer 14-1	$Al_{0.3}Ga_{0.7}As$	400	Zn	2×10^{18}	2×10^{18}
Layer 12	GaAs	500	Zn	2×10^{18}	2×10^{18}
Substrate 10	GaAs				

While a p-type substrate is used in the sixth and seventh embodiments, an n-type substrate may be used. In this case, the impurity concentration of the anode layer may be lower than that of an n-type gate layer. Also, while the embodiments are illustrated for an impurity Zn which may be easily diffused, the present invention may be applicable to another kind of impurities for the fifth and sixth layers.

Eighth Embodiment

Three fundamental structures of self-scanning light-emitting device to which the light-emitting thyristor of the

present invention can be applied will now be described.

Fig.22 shows an equivalent circuit diagram of a first fundamental structure of the self-scanning light-emitting device. According to the structure, light-emitting thyristors ··· T_{-2}, T_{-1}, T_0, T_{+1}, T_{+2}··· are used as light-emitting elements, each of thyristors comprising gate electrodes ··· G_{-2}, G_{-1}, G_0, G_{+1}, G_{+2}···, respectively. Supply voltage V_{GK} is applied to all of the gate electrodes via a load resistor R_L, respectively. The neighboring gate electrodes are electrically connected to each other via a resistor R_I to obtain interaction. Each of three transfer clock (ϕ_1, ϕ_2, ϕ_3) lines is connected to the anode electrode of each light-emitting element at intervals of three elements (in a repeated manner).

The operation of this self-scanning light-emitting device will now be described. Assume that the transfer clock ϕ_3 is at a high level, and the light-emitting thyristor T_0 is turned on. At this time, the voltage of the gate electrode G_0 is lowered to a level near zero volts due to the characteristic of the light-emitting thyristor. Assuming that the supply voltage V_{GK} is 5 volts, the gate voltage of each light-emitting thyristor is determined by the resistor network consisting of the load resistors R_L and the interactive resistors R_I. The gate voltage of a thyristor near the light-emitting thyristor T_0 is lowered most, and the gate voltage V(G) of each subsequent thyristor rises as it is remote from the thyristor T_0. This can be expressed as follows:

$$V(G_0)<V(G_{+1})=V(G_{-1})<V(G_{+2})=V(G_{-2})\cdots\cdots\cdots(1)$$

The difference among these voltages can be set by properly

selecting the values of the load resistor R_L and the interactive resistor R_I.

It is known that the turn-on voltage V_{ON} of the light-emitting thyristor is a voltage that is higher than the gate voltage V(G) by the diffusion potential V_{dif} of pn junction as shown in the following formula.

$$V_{ON} \fallingdotseq V(G)+V_{dif} \quad \cdots\cdots\cdots (2)$$

Consequently, by setting the voltage applied to the anode to a level higher than this turn-on voltage V_{ON}, the light-emitting thyristor may be turned on.

In the state where the light-emitting thyristor T_0 is turned on, the next transfer clock ϕ_1 is raised to a high level. Although this transfer clock ϕ_1 is applied to the light-emitting thyristors T_{+1} and T_{-2} simultaneously, only the light-emitting thyristor T_{+1} can be turned on by setting the high-level voltage V_H of the transfer clock ϕ_1 to the following range.

$$V(G_{-2})+V_{dif} > V_H > V(G_{+1})+V_{dif} \quad \cdots\cdots\cdots (3)$$

By doing this, the light-emitting thyristors T_0 and T_{+1} are turned on simultaneously. When the transfer clock ϕ_3 is lowered to a low level, the light-emitting thyristors T_0 is turned off, and this completes transferring ON state from the thyristor T_0 to the thyristor T_{+1}.

Based on the principle described above, the ON state of the light-emitting thyristor is sequentially transferred by setting the high-level voltage of the transfer clocks ϕ_1, ϕ_2 and ϕ_3 in such a manner as to overlap sequentially and slightly with each other. In this way, the self-scanning light-emitting device according to the present invention is accomplished.

Fig.23 shows an equivalent circuit diagram of a second fundamental structure of the self-scanning light-emitting device. This self-scanning light-emitting device uses a diode as means for electrically connecting the gate electrodes of light-emitting thyristors to each other. That is, the diodes $\cdots D_{-2}, D_{-1}, D_0, D_{+1} \cdots$ are used in place of the interactive resistors R_I in Fig.22. The number of transfer clock lines may be only two due to the unidirectional of diode characteristics, then each of two clock (ϕ_1 , ϕ_2) lines is connected to the anode electrode of each light-emitting element at intervals of two elements.

The operation of this self-scanning light-emitting device will now be described. Assuming that as the transfer clock ϕ_2 is raised to a high level, the light-emitting thyristor T_0 is turned on. At this time, the voltage of the gate electrode G_0 is reduced to a level near zero volts due to the characteristic of the thyristor. Assuming that the supply voltage V_{GK} is 5 volts, the gate voltage of each light-emitting thyristor is determined by the network consisting of the load resistors R_L and the diodes D. The gate voltage of an thyristor nearest to the light-emitting thyristor T_0 drops most, and the gate voltages of those thyristors rise as they are further away from the light-emitting thyristor T_0.

The voltage reducing effect works only in the rightward direction from the light-emitting thyristor T_0 due to the unidirectionality and asymmetry of diode characteristics. That is, the gate electrode G_{+1} is set at a higher voltage with respect to the gate electrode G_0 by a forward rise voltage V_{dif} of the diode, while the gate electrode G_{+2} is set

at a higher voltage with respect to the gate electrode G_{+1} by a forward rise voltage V_{dif} of the diode. On the other hand, current does not flow in the diode D_{-1} on the left side of the light-emitting thyristor T_0 because the diode D_{-1} is reverse-viased. As a result, the gate electrode G_{-1} is at the same potential as the supply voltage V_{GK}.

Although the next transfer clock ϕ_1 is applied to the nearest light-emitting thyristor T_{+1}, T_{-1}; T_{+3}, T_{-3}; and so on, the thyristor having the lowest turn-on voltage among them is T_{+1}, whose turn-on voltage is approximately the gate voltage of G_{+1} + V_{dif}, about twice as high as V_{dif}. The thyristor having the second lowest turn-on voltage is T_{+3}, about four times as high as V_{dif}. The turn-on voltage of the thyristors T_{-1} and T_{-3} is about V_{GK} + V_{dif}.

It follows from the above discussion that by setting the high-level voltage of the transfer clock ϕ_1 to a level about twice to four times as high as V_{dif}, only the light-emitting thyristor T_{+1} can be turned-on to perform a transfer operation.

Fig.24 shows an equivalent circuit diagram of a third fundamental structure of the self-scanning light-emitting device. According to the structure, a transfer portion 40 and a light-emitting portion 42 are separated. The circuit structure of the transfer portion 40 is the same as that shown in Fig.23, and the light-emitting thyristors $\cdots T_{-1}$, T_0, T_{+1}, $T_{+2}\cdots$ are used as transfer elements in this embodiment.

The light-emitting portion 42 comprises writable light-emitting elements L_{-1}, L_0, L_{+1}, $L_{+2}\cdots$, each gate thereof is connected to the gate $\cdots G_{-1}$, G_0, $G_{+1}\cdots$ of the transfer elements $\cdots T_{-1}$, T_0, T_{+1}, T_{+2}, respectively. A write signal S_{in} is applied

to all of the anode of the writable light-emitting elements.

In the following, the operation of this self-scanning light-emitting device will be described. Assuming that the transfer element T_0 is in the ON state, the voltage of the gate electrode G_0 lowers below the supply voltage V_{GK} and to almost zero volts. Consequently, if the voltage of the write signal S_{in} is higher than the diffusion potential (about 1 volt) of the pn junction, the light-emitting element L_0 can be turned into a light-emission state.

On the other hand, the voltage of the gate electrode G_{-1} is about 5 volts, and the voltage of the gate electrode G_{+1} is about 1 volt. Consequently, the write voltage of the light-emitting element L_{-1} is about 6 volts, and the write voltage of the light-emitting element L_{+1} is about 2 volts. It follows from this that the voltage of the write signal S_{in} which can write only in the light-emitting element L_0 is a range of about 1-2 volts. When the light-emitting element L_0 is turned on, that is, in the light-emitting state, the voltage of the write signal S_{in} is fixed to about 1 volt. Thus, an error of selecting other light-emitting elements can be prevented.

Light emission intensity is determined by the amount of current fed to the write signal S_{in}, an image can be written at any desired intensity. In order to transfer the light-emitting state to the next element, it is necessary to first turn off the element that is emitting light by temporarily reducing the voltage of the write signal S_{in} down to zero volts.

INDUSTRIAL APPLICABILITY

According to the present invention, a light-emitting

thyristor having an improved luminous efficiency may be provided, and furthermore a self-scanning light-emitting device composed of an array of light-emitting thyristors of the present invention and having a self-scanning function may be provided.

CLAIMS

1. A light-emitting thyristor, comprising :

a GaAs substrate ; and

a GaAs buffer layer provided on the GaAs substrate ; and four layers consisting of a first conductivity type of AlGaAs layer and a second conductivity type of AlGaAs layer stacked alternately on the buffer layer;

wherein the AlGaAs layer just above the buffer layer is composed of a plurality of AlGaAs layers, Al compositions thereof being increased upward in steps.

2. The light-emitting thyristor of claim 1, wherein a quantum well layer or a strained superlattice structure is inserted into the uppermost layer of the plurality of AlGaAs layers.

3. A light-emitting thyristor, comprising :

a GaAs substrate ; and

a GaAs buffer layer provided on the GaAs substrate ; and four layers consisting of a first conductivity type of AlGaAs layer and a second conductivity type of AlGaAs layer stacked alternately on the buffer layer;

wherein the Al composition of the AlGaAs layer just above the buffer layer is increased upward continuously.

4. The light-emitting thyristor of claim 3, wherein a quantum well layer or a strained superlattice structure is inserted into the AlGaAs layer just above the buffer layer.

5. A light-emitting thyristor, comprising :

a GaAs substrate ;

a GaAs buffer layer provided on the GaAs substrate ; and

four layers consisting of a first conductivity type of AlGaAs layer and a second conductivity type of AlGaAs layer stacked alternately on the buffer layer;

wherein a quantum well layer on a strained superlattice structure is inserted between the buffer layer and the AlGaAs layer just above the buffer layer, or into the AlGaAs layer just above the buffer layer.

6. A light-emitting thyristor, comprising :

a substrate ; and

four layers consisting of a first conductivity type of semiconductor layer and a second conductivity type of semiconductor layer stacked alternately on the substrate; and

wherein an uppermost layer from which light is emitted comprises material selected from a group consisting of InGaP, InGaAsP, and AlGaInP.

7. The light-emitting thyristor of claim 6, wherein the composition of the selected material is adjusted so as to be lattice matched with the material of the substrate.

8. The light-emitting thyristor of claim 7, wherein the material of the substrate is GaAs.

9. A light-emitting thyristor, comprising :

a p-type anode layer ;

an n-type gate layer formed adjacent to the p-type anode layer ;

a p-type layer formed adjacent to the n-type gate

layer ; and

an n-type cathode layer formed adjacent to the p-type gate layer ;

wherein an impurity concentration of at least the part of the anode layer near the n-type gate layer is lower than an impurity concentration of the n-type gate layer.

10. The light-emitting thyristor of claim 9, wherein the impurity of the anode layer is Zn.

11. The light-emitting thyristor of claim 9, wherein the impurity of the anode layer is Zn, and the impurity of the n-type gate is Si.

12. A self-scanning light-emitting device, comprising:

a structure in which a plurality of light-emitting elements each having a control electrode for controlling threshold voltage or current for light-emitting operation are arranged, the control electrodes of the light-emitting elements are connected to the control electrode of at least one light-emitting element located in the vicinity thereof via an interactive resistor, and a plurality of wirings to which voltage or current is applied are connected to electrodes for controlling the light emission of light-emitting elements,

wherein the light-emitting element is a light-emitting thyristor as set forth in any one of claims 1-11.

13. A self-scanning light-emitting device, comprising:

a structure in which a plurality of light-emitting

elements each having a control electrode for controlling threshold voltage or current for light-emitting operation are arranged, the control electrodes for the light-emitting elements are connected to the control electrode of at least one light-emitting element located in the vicinity thereof via an electrically unidirectional element, and a plurality of wiring to which voltage or current is applied are connected to electrodes for controlling the light emission of light-emitting elements,

wherein the light-emitting element is a light-emitting thyristor as set forth in any one of claims 1-11.

14. The self-scanning light-emitting device of claim 13, wherein the electrically unidirectional element is a diode.

15. A self-scanning light-emitting device, comprising :

a self-scanning transfer element array having such a structure that a plurality of transfer elements each having a control electrode for controlling threshold voltage or current for transfer operation are arranged, the control electrodes of the transfer elements are connected to the control electrode of at least one transfer element located in the vicinity thereof via an interactive resistor, power-supply lines are connected to the transfer elements by electrical means, and clock lines are connected to the transfer elements, and

a light-emitting element array having such a structure that a plurality of light-emitting elements each having a control electrode for controlling threshold voltage or current are arranged, the control electrodes of the light-

emitting element array are connected to the control electrodes of said transfer elements by electrical means, and lines for applying current for light emission of the light-emitting element are provided,

wherein the light-emitting element is a light-emitting thyristor as set forth in any one of claims 1-11.

16. A self-scanning light-emitting device, comprising :

a self-scanning transfer element array having such a structure that a plurality of transfer elements each having a control electrode for controlling threshold voltage or current for transfer operation are arranged, the control electrodes of the transfer elements are connected to the control electrode of at least one transfer element located in the vicinity thereof via an electrically unidirectional element, power-supply lines are connected to the transfer elements by electrical means, and clock lines are connected to the transfer elements, and

a light-emitting element array having such a structure that a plurality of light-emitting elements each having a control electrode for controlling threshold voltage or current are arranged, the control electrodes of the light-emitting element array are connected to the control electrodes of said transfer elements by electrical means, and lines for applying current for light emission of the light-emitting element are provided,

wherein the light-emitting element is a light-emitting thyristor as set forth in any one of claims 1-11.

17. The self-scanning light-emitting device of claim 16,

wherein the electrically unidirectional element is a diode.

ABSTRACT

A light-emitting thyristor having an improved luminous efficiency is provided. According to the light-emitting thyristor, a p-type AlGaAs layer and an n-type AlGaAs layer are alternately stacked to form a pnpn structure on a GaAs buffer layer formed on a GaAs substrate, and Al composition of the AlGaAs layer just above the GaAs buffer layer is increased in steps or continuously.

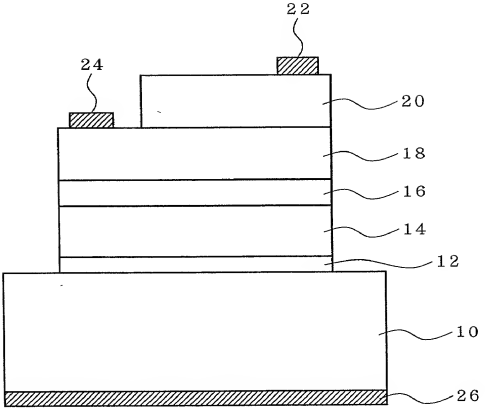
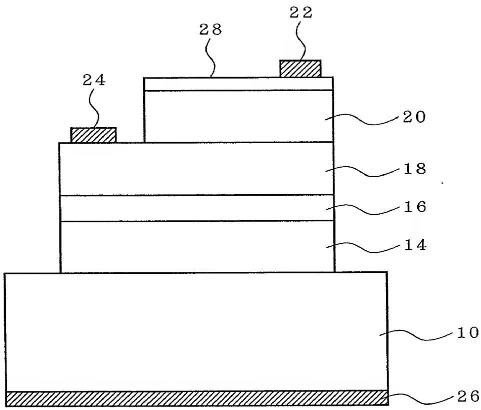
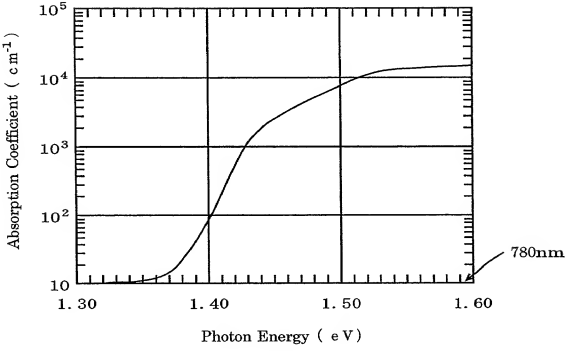


FIG. 1



F I G. 2


Absorption Coefficient (cm^{-1})
10^5
10^4
10^3
10^2
10
1. 30
1. 40
1. 50
1. 60
780nm
Photon Energy (eV)

F I G. 3

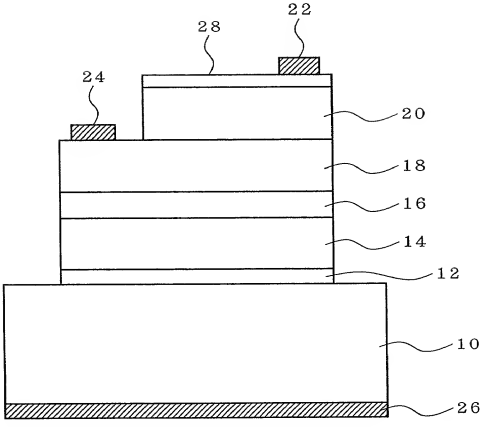


FIG. 4

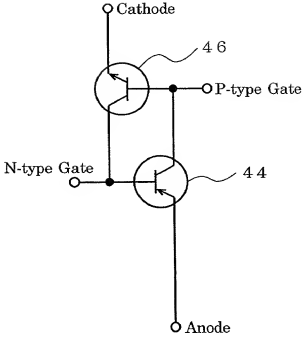

Cathode
46
P-type Gate
N-type Gate
44
Anode

FIG. 5

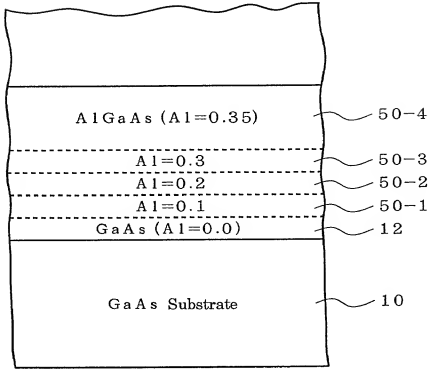

AlGaAs (Al=0.35)
50-4
Al=0.3
50-3
Al=0.2
50-2
Al=0.1
50-1
GaAs (Al=0.0)
12
GaAs Substrate
10

FIG. 6

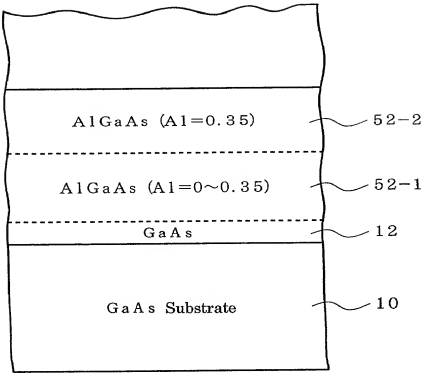

AlGaAs (Al=0.35)
52-2
AlGaAs (Al=0~0.35)
52-1
GaAs
12
GaAs Substrate
10

FIG. 7

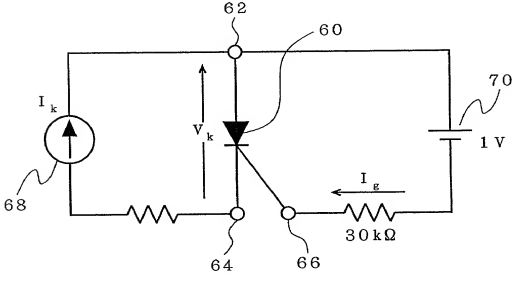

62
60
70
I_k
V_k
1V
I_g
68
30kΩ
64
66

FIG. 8

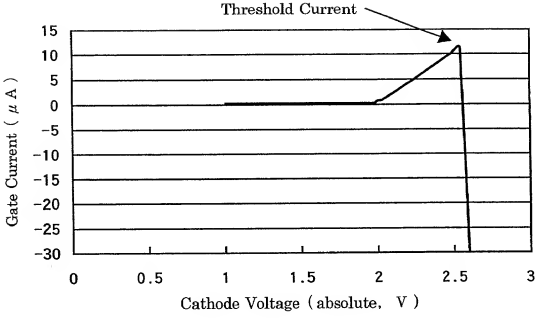

Threshold Current
15
10
5
0
−5
−10
−15
−20
−25
−30
Gate Current (μA)
0
0.5
1
1.5
2
2.5
3
Cathode Voltage (absolute, V)

FIG. 9

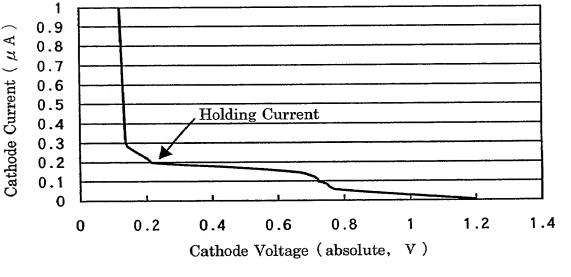

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Cathode Current (μA)
Holding Current
0
0.2
0.4
0.6
0.8
1
1.2
1.4
Cathode Voltage (absolute, V)

FIG. 10

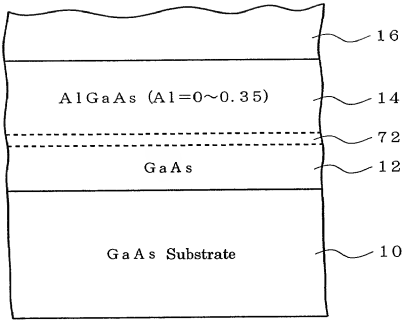

16
AlGaAs (Al=0~0.35)
14
72
GaAs
12
GaAs Substrate
10

FIG. 11

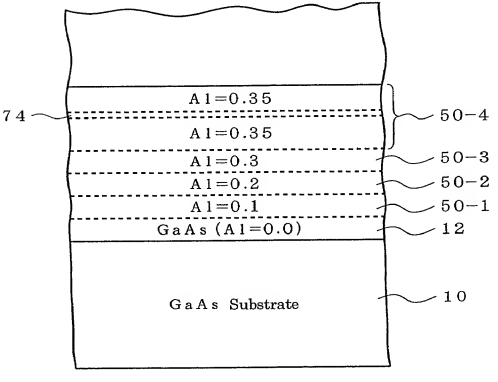

74
Al=0.35
Al=0.35
50-4
Al=0.3
50-3
Al=0.2
50-2
Al=0.1
50-1
GaAs (Al=0.0)
12
GaAs Substrate
10

FIG. 12

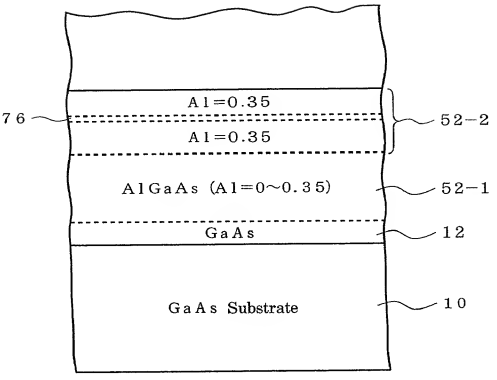

Al=0.35
76
Al=0.35
52-2
AlGaAs (Al=0~0.35)
52-1
GaAs
12
GaAs Substrate
10

FIG. 13

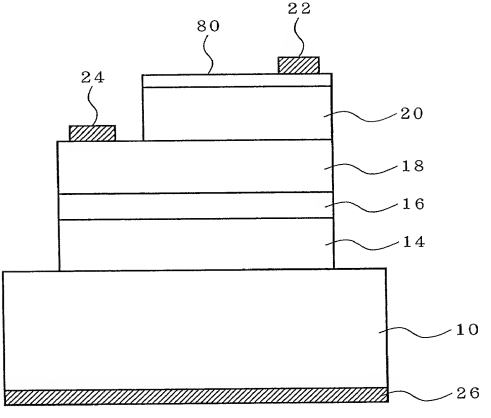

22
80
24
20
18
16
14
10
26

FIG. 14

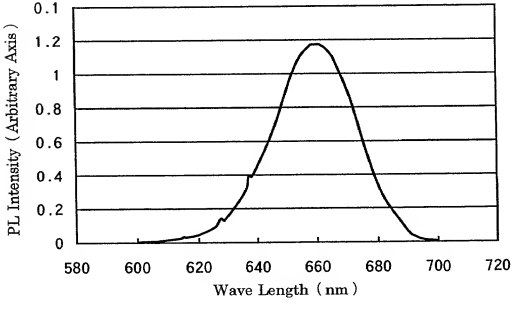

0.1
1.2
1
0.8
0.6
0.4
0.2
0
PL Intensity (Arbitrary Axis)
580
600
620
640
660
680
700
720
Wave Length (nm)

FIG. 15

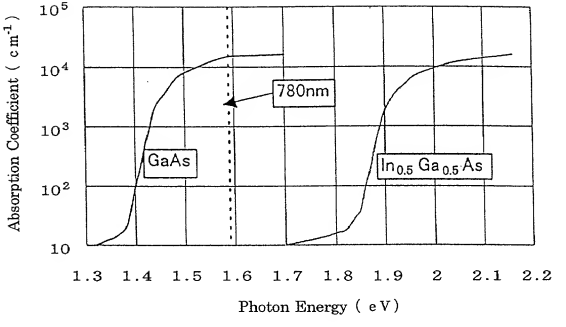

Absorption Coefficient (cm-1)
10^5
10^4
10^3
10^2
10
780nm
GaAs
In0.5 Ga0.5 As
1.3 1.4 1.5 1.6 1.7 1.8 1.9 2 2.1 2.2
Photon Energy (eV)

FIG. 16

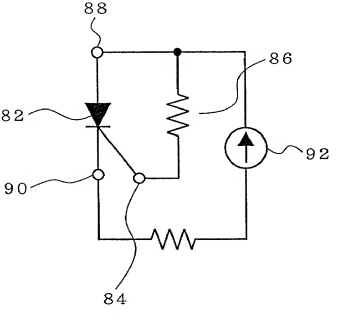

88
86
82
92
90
84

FIG. 17

InGaP lattice matched with GaAs
(2.261eV)
GaP
1.0
0.8
0.6
0.4
0.2
0
x
(1.35eV)
InP
1.0
0.8
0.6
0.4
0.2
0
y
InAs
(0.360eV)
GaAs
(1.424eV)
lattice coefficient of GaAs
102
100 (About 780nm)
5.50A
5.55A
5.60A
5.65A
5.70A
5.75A
5.80A
5.85A
InP=5.87A
5.90A
5.95A
6.00A
0.2eV
0.5
0.6
0.7
0.8
1.0
1.2
1.3
1.4
1.5
1.6
1.7
1.8
2.0
2.2

FIG. 18

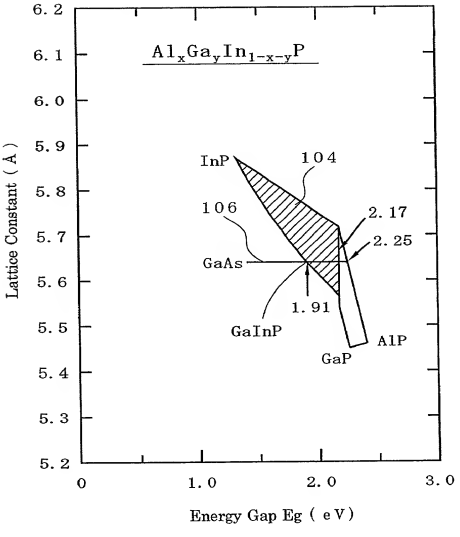

$Al_xGa_yIn_{1-x-y}P$
Lattice Constant (Å)
Energy Gap Eg (eV)
6.2
6.1
6.0
5.9
5.8
5.7
5.6
5.5
5.4
5.3
5.2
0
1.0
2.0
3.0
InP
104
106
2.17
2.25
GaAs
1.91
GaInP
AlP
GaP

FIG. 19

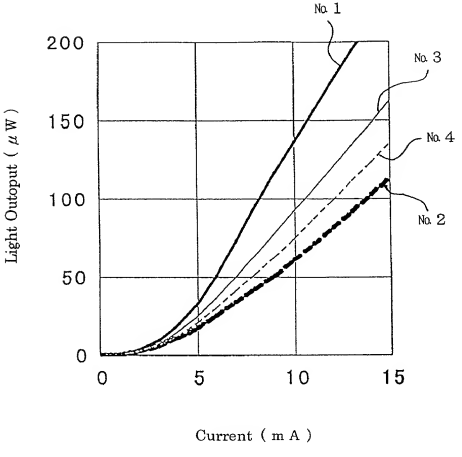

No. 1
No. 3
No. 4
No. 2
200
150
100
50
0
0
5
10
15
Light Outoput (μW)
Current (mA)

FIG. 20

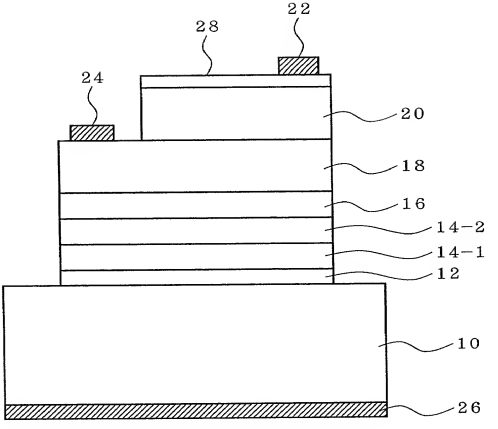


FIG. 21

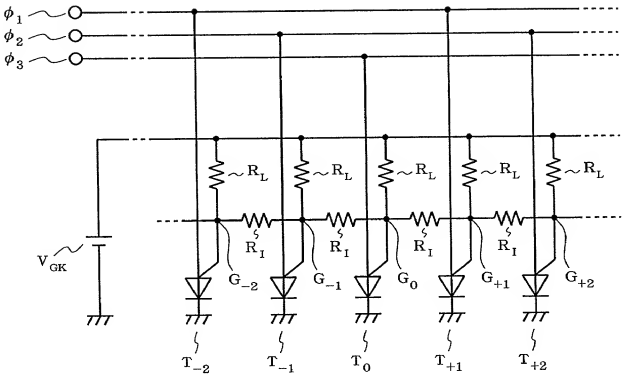


FIG. 22

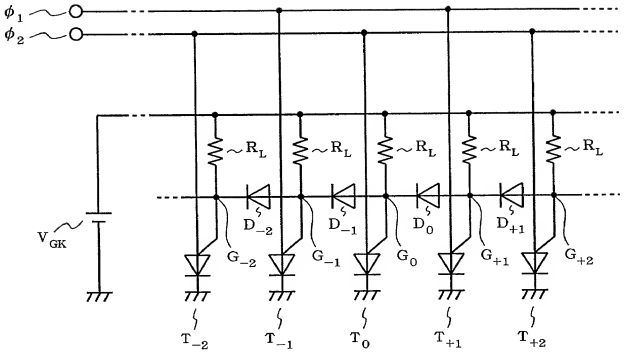


FIG. 23

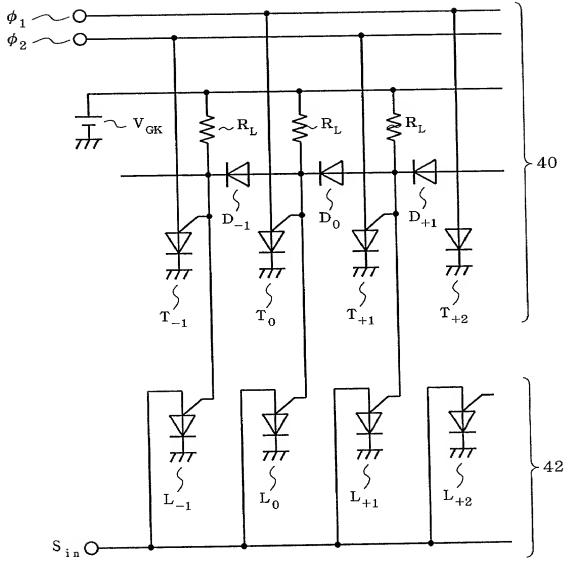


FIG. 24

Declaration and Power of Attorney For Patent Application
English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
LIGHT-EMITTING THYRISTOR AND SELF-SCANNING LIGHT-EMITTING DEVICE,
the specification of which is attached hereto unless the following box is checked:

☐ was filed on 14/08/2000 as
United States Application Number or PCT International Application Number PCT/JP00/05442
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
11-234,881	JAPAN	23/08/1999	☐
(Number)	(Country)	(Day/Month/Year Filed)	
11-234,884	JAPAN	23/08/1999	☐
(Number)	(Country)	(Day/Month/Year Filed)	
11-238,110	JAPAN	25/08/1999	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

100 Full name of sole or first inventor (given name, family name) Nobuyuki KOMABA

Inventor's signature Nobuyuki Komaba Date April 2, 2001

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Second Inventor's signature Seiji Ohno Date April 2, 2001

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☐ Additional inventors are being named on separately numbered sheets attached hereto.